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S/N 10/775,656 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yamashita et al	Examiner:	Dinh
Serial No.:	10/775,656	Group Art Unit:	2841
Filed:	February 9, 2004	Docket No.:	10873.1397US01
Title:	ELECTRONIC COMPONENT BUILT-IN MODULE AND METHOD OF MANUFACTURING THE SAME		

CERTIFICATE UNDER 37 CFR 1.6(d):
I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on February 28, 2007.

By _____
Name: Gina M. Dahl

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR PRE-APPEAL BRIEF REVIEW

Dear Sir:

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request. The review is requested for the reasons stated on the attached sheets titled "Reasons In Support Of Request for Pre-Appeal Brief Review".

This request is being filed with a notice of appeal.

Respectfully submitted,

HAMRE, SCHUMANN, MUELLER & LARSON, P.C.
P.O. Box 2902
Minneapolis, MN 55402-0902
(612)455-3800

Dated: February 28, 2007 By _____
Douglas P. Mueller
Reg. No. 30,300

DPM

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REASONS IN SUPPORT OF REQUEST FOR PRE-APPEAL BRIEF REVIEW

Dear Sir:

Applicants request review of the October 31, 2006 final rejection of the above application. The sole issue raised in the final rejection is a rejection of claims 1-17 as being unpatentable over Nakatani (US 6,038,133) in view of Ozawa (US 5,172,304). Applicants respectfully contend that the rejection is based on a clearly erroneous interpretation of the present claims and the references, and should be withdrawn.

Claim 1 requires a pair of opposed circuit substrates with an insulating layer disposed therebetween. An inner via, which connects wiring patterns on the opposed substrates, is provided in the insulating layer. An electronic component is embedded in the insulating layer. The substrates include an insulating base material containing a resin, and the insulating layer contains an inorganic filler and a resin composition containing a thermosetting resin. The glass transition temperature of the resin contained in the insulating layer (Tg1 in claim 1) is higher

than the glass transition temperature of the resin of the insulating base material of the circuit substrates (Tg2 in claim 1). Similar features are presented in the independent method claim 9.

The requirement of the different glass transition temperatures is significant. When the insulating layer has a larger coefficient of expansion than the circuit substrate, the circuit substrates will tend to block the expansion of the insulating layer in the lateral direction as the temperature is increased. As a result, the insulating layer will tend to expand in the thickness direction. The expansion in the thickness direction can put stress on the conductive material used for the inner via connecting the opposed circuit substrates. This can result in separation of the conductive material and loss of conductivity in the inner via. The problem is particularly pronounced in a product including an electronic component embedded in the insulating layer. In such products the insulating layer must be relatively thick to accommodate the electronic component, and the relatively large thickness of the insulating layer, which corresponds to the length dimension of the inner via, results in a relatively large aspect ratio (length/diameter) for the inner via. This makes the inner via more susceptible to damage and loss of conductivity when the thickness of the insulating layer expands. The higher glass transition temperature for the resin in the composition of the insulating layer promotes the ability of that resin to expand laterally, thus alleviating the pressure exerted in the thickness direction (the longitudinal direction of inner via). The experimental results reported at pages 24-26 of the present specification and the accompanying tables and figures show how the different glass transition temperatures required by the invention of claim 1 alleviate this problem and advantageously improve the reliability of the product.

Neither Nakatani nor Ozawa nor their combination teaches or suggest the invention of claims 1 and 9. Specifically, neither Nakatani nor Ozawa specifies the use of different resins for the circuit substrates and insulating layer, and therefore cannot suggest the particular glass transition temperature relationship for the resins required by claims 1 and 9.

Col. 7, lines 10-14 of Nakatani discuss various types of resins that could be used. However, the reference does not discuss using different materials for different layers nor the selection of materials to meet glass transition temperature relationship required by claims 1 and 9. The rejection seems to recognize this point.

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Office Action Dated May 17, 2006

The rejection (page 3, second paragraph) relies on Ozawa to teach the relationship between the glass transition temperatures Tg1 and Tg2. More specifically, the rejection contends that since the dielectric substrate (2) taught by Ozawa includes a mixture of dielectric powder and resin, the Tg of the dielectric substrate (2) must be higher than the Tg of each of the resin substrates. Applicants respectfully submit that the rejection's reasoning is erroneous. Tg is a physical property of a particular resin. The presence or absence of filler has no effect on the glass transition temperature. Note that in the Examples in the present specification, the same inorganic filler was used in the same amounts, but different glass transition temperatures were present because different resins were used. Ozawa provides no discussion whatsoever of using different resins in its layers 2 and 6, and therefore, like Nakatani, fails to suggest the selection of resins for the insulating base material of the circuit substrates and the insulating layer that would satisfy the glass transition temperature relationship required by claims 1 and 9.

In view of the above, Applicants submit that the rejection is clearly erroneous and should be withdrawn.

Respectfully submitted,

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